design ideas

Edited by Bill Travis and Anne Watson Swager

Circuit monitors quad supply for PCI systems

Roger Zemke, Linear Technology Corp, Milpitas, CA

Many modern systems operate with multiple power supplies that must meet tight tolerances to accommodate high-end µPs and peripherals. For instance, PCI applications may use as many as four supplies: 5V, 3.3V, and ±12V. The circuit in **Figure 1** can monitor all these voltages for an undervoltage condition and can also monitor the three positive voltages for an overvoltage condition. The LTC1536 has a built-in ability to monitor the 3.3 and 5V levels and one adjustable level for undervoltage conditions. The adjustable input of the IC monitors the 12V supply. The LTC1536 also acts as the logic input for the open-drain outputs of the LTC1444 quad comparator.

Comparators A, B, and C of the LTC1444, along with resistors R_1 through R_6, monitor the 3.3, 5, and 12V positive supplies, respectively, for an overvoltage condition. The nominal overvoltage trip points are 3.61, 5.28, and 12.6V. Comparator D, aided by resistors R_7 and R_8, monitors the −12V supply for an undervoltage condition. The nominal trip point for the −12V supply is 10.8V. The open-drain outputs of all the comparators, tied together, connect to the adjustable input of the LTC1536. The resistor divider comprising R_9 and R_{10} provides a pull-up function for the open-drain outputs. The divider also sets up the 12V undervoltage trip point, which is nominally 11.3V. A Schottky diode tied to the LTC1536's adjustable input can provide another logic input, such as a Power-Good signal. If any undervoltage or overvoltage fault conditions occur, the LTC-1536 issues a reset until 200 msec after the fault condition goes away. (DI #2403).

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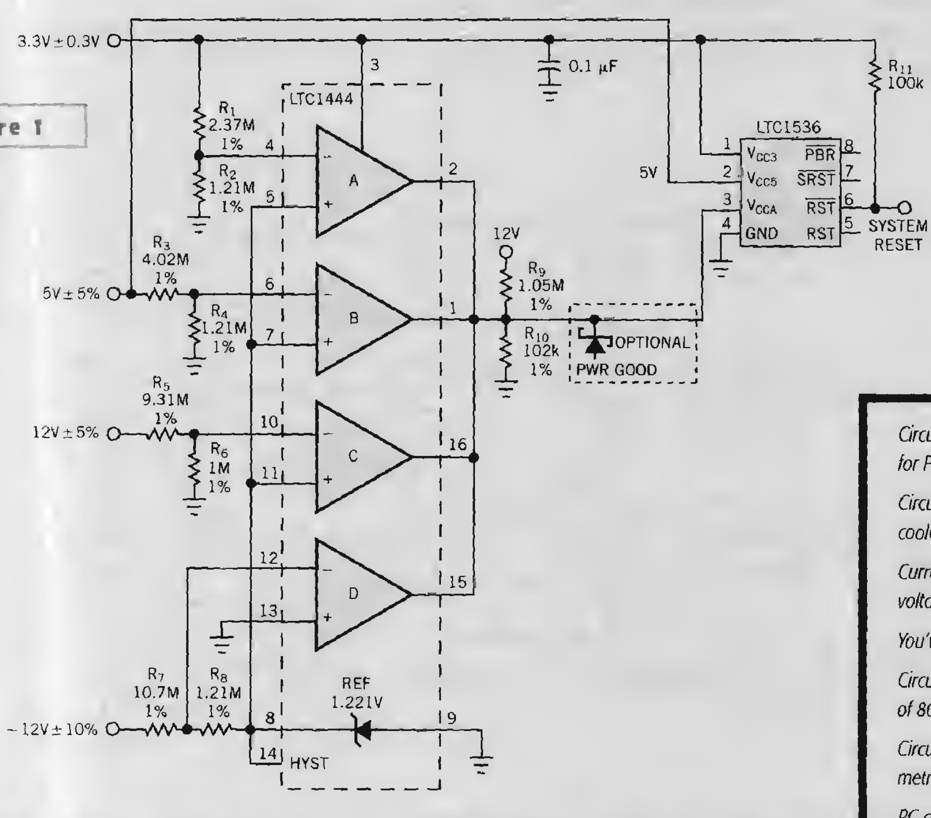
Figure 1



Two ICs monitor PCI-system quad supplies for undervoltage and overvoltage fault conditions.

Circuit controls multiple thermoelectric coolers

By Frank Effenberger, Bellcore, Morristown, NJ

Optoelectronic and other components sometimes use a thermoelectric cooler and a thermistor for temperature control. A typical thermoelectric cooler has 1A maximum current and 1Ω impedance. These parameters make simple series-pass drive circuits inefficient, given the typical available supply voltages (5, 12, or 15V). Often, several thermoelectric coolers exist in a single circuit (for example, a multiple-wavelength optical transmitter). In this case, you can obtain improved efficiency by using the circuit in **Figure 1**. This circuit has three devices to cool, so it contains three coolers and three thermistors. On the sensor side, each thermistor connects to a standard proportional-integral-differential op-amp or µP-based-controller circuit. Each controller produces a command voltage that is proportional to the current its respective cooler requires.

The command voltages drive precision rectifier circuits (op amps IC_1 to IC_3) that generate the maximum control V_{MAX}. Op amp IC_4 limits V_{MAX}, thus allowing you to control the maximum current delivered to the coolers. This limited output, V_{LIM}, is the input to the main transistor-driver amplifier, IC_8. V_{LIM} commands the main transistor to pass a current corresponding to the largest demand, subject to the limit constraint. The thermoelectric coolers connect in series, and this chain receives its current via the main series-pass transistor Q_4. IC_8 drives this transistor such that the voltage drop across R_{SENSE} equals V_{LIM}. You choose R_{SENSE} to equal the impedance of one cooler. The coolers have shunt transistors (Q_1 through Q_3) that divert any excess current around the individual coolers. The shunt transistors receive their drive from op amps IC_5 through IC_7, which are connected as difference amplifiers. The op amps drive the shunt transistors such that the voltage across each thermoelectric cooler equals the command voltage for that cooler.

Because the sense resistance equals that of the coolers, the current passing through each cooler assumes the correct value. The actual values of the difference-amplifier resistors, R, and the transistor-base resistors depend on the type of op amps and transistors you select. In most cases, the desired cooler currents have an average value, I_{MEAN}, and a maximum value, I_{MAX}, that are almost equal. If you cool N coolers using separate circuits, the supply needs to deliver $N \times I_{MEAN}$A. Using the series-connected circuit, the supply current reduces to just I_{MEAN}. Even in the case in which you an optimize the supply voltage for either circuit, the power dissipation for the series-connected circuit is lower because it drops a smaller fraction of the supply voltage through the series-pass transistor. (DI #2395).

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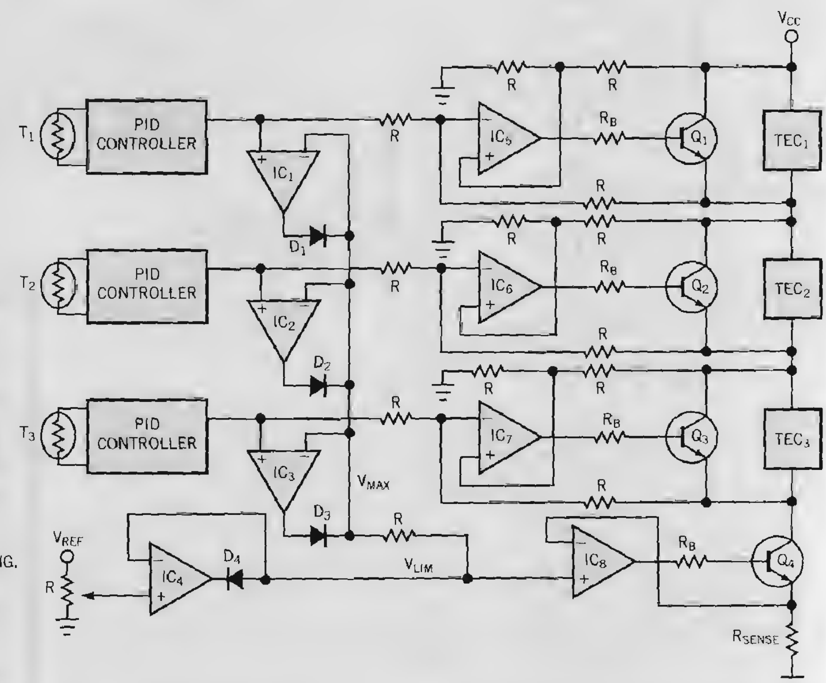
Figure 1



NOTES:
R=10 kΩ, R_B=1 kΩ, R_{SENSE}=1Ω.
IC_1 THROUGH IC_8=¼ TL084 QUAD OP AMP.
Q_1 THROUGH Q_4=TIP120 DARLINGTON TRANSISTOR.
D_1 THROUGH D_4=1N914.
T_1 THROUGH T_3=10k AT 20°C.
TEC_1 THROUGH TEC_3=1A AT 1V FULL RATING.
PID BLOCK IS A GENERIC RESISTANCE-INPUT AND VOLTAGE-OUTPUT ANALOG CONTROL CIRCUIT.

A series connection of thermoelectric coolers provides more efficient temperature control and fewer supply-current requirements than circuits using individual cooler controllers.

Current-input ADC measures voltages

Jim Todsen, Burr-Brown Corp, Tuscon, AZ

A practical realization of a spread-spectrum technique lowers a μP's clock-related EMI by approximately 4 dB without the drawbacks associated with modulation (**Figure 1**). The spread-spectrum technique is a popular method to reduce μP-clock-related EMI (**Reference 1**). Using this method, the μP's clock frequency constantly shifts around and creates a moving target for quasipeak EMI detection. Although this method dramatically reduces measured EMI, it has a few drawbacks.

The first drawback is an unpredictable clock frequency. Peripheral devices that share the same clock with the μP and rely on a stable clock frequency might suffer. One example is an ADC that relies on direct μP control to define the sampling time. The second drawback is the periodic nature of the frequency shift. The technique essentially modulates the clock frequency with an approximately 50-kHz frequency. This frequency is slightly higher than the audio band to prevent audio "hum." In some systems, however, this 50-kHz modulation frequency may be in band with data-acquisition or other sensitive analog circuitry. Under these circumstances, separate nonmodulated digital-control and clock signals are necessary to prevent demodulation of 50-kHz frequency and to prevent analog noise.

Consider the product of two square signals with unity amplitude, $x_1(t)$ and $x_2(t)$, where $x_1(t)$ is a square signal with frequency ω_1 and $x_2(t)$ is a square signal with frequency ω_2 in radians (**Figure 2a**). The Fourier transforms of square waves $x_1(t)$ and $x_2(t)$ are:

$$x_1(t)=\frac{4}{\pi}\left[\sin(\omega_1)+\frac{\sin(3\omega_1)}{3}+\frac{\sin(5\omega_1)}{5}+\cdots\right], \text{and}$$

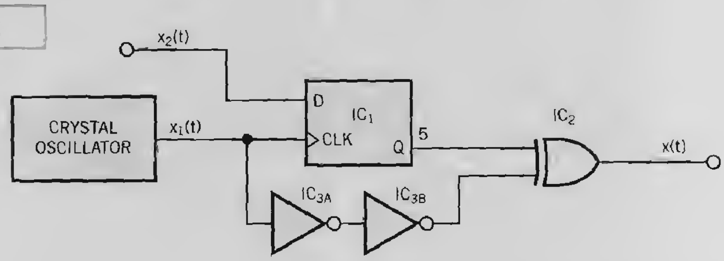
$$x_2(t)=\frac{4}{\pi}\left[\sin(\omega_2)+\frac{\sin(3\omega_2)}{3}+\frac{\sin(5\omega_2)}{5}+\cdots\right].$$

The Fourier transform of the product of x_1t and x_2t is:

$$x(t)=x_1(t)x_2(t)=\frac{4}{\pi}\left[\sin(\omega_1)\sin(\omega_2)+\frac{\sin(3\omega_1)\sin(\omega_2)}{3}+\cdots+\frac{\sin(3\omega_2)\sin(\omega_1)}{3}+\cdots\right].$$

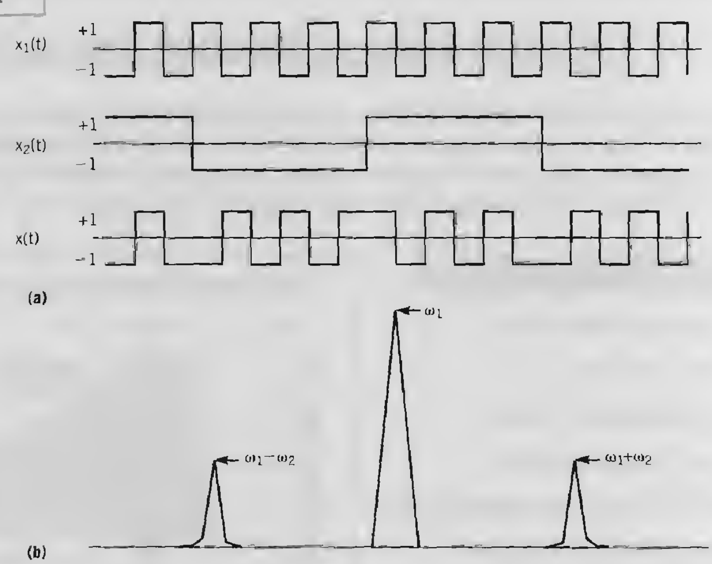
You can limit the series to the first term

Figure 1



Simple logic gates implement a spread-spectrum technique that produces predictable clock behavior and introduces no unwanted modulation frequencies.

Figure 2



Multiplying $x_1(t)$ by $x_2(t)$ produces x(t) (a). In the frequency domain, the multiplication causes the original main frequency component, ω_1, to split into two equal components (b).

for simplification:

$$x(t)=\frac{4}{\pi}\sin(\omega_1)\sin(\omega_2)=$$

$$\frac{4}{\pi}\left[\frac{1}{2}\cos(\omega_1-\omega_2)-\frac{1}{2}\cos(\omega_1-\omega_2)\right].$$

If ω_1 is the frequency of the crystal oscillator and ω_2 is the result of the frequency division of ω_1 by 128, for example, then you can rewrite the previous equation as follows:

$$x(t)=\frac{4}{\pi}\sin(\omega_1)\sin\left(\frac{\omega_1}{128}\right)=$$

$$\frac{4}{\pi}\left[\frac{1}{2}\cos\left(\omega_1-\frac{\omega_1}{128}\right)-\frac{1}{2}\cos\left(\omega_1+\frac{\omega_1}{128}\right)\right].$$

In other words, the frequency peak of $x_1(t)$ multiplied by $x_1(t)/128$ splits into two frequency peaks separated by $2\times \omega_1/128$. Each peak has half of the energy of the original ω_1 peak. **Figure 2b** shows a Matlab-generated spectrum of $x_1(t)$ and $x(t)$.

Multiplying the nth harmonic of the original $x_1(t)$ signal by x_2t splits the nth harmonic into two major frequency components with frequencies $n\times\omega_1+\omega_1/128$ and $n\times\omega_1-\omega_1/128$. (These product terms are the most significant.) If $x_2(t)$ is purely sinusoidal and the frequency analyzer has an unlimited narrow frequency bandwidth, the initial $x_1(t)$ nth harmonic splits into two frequency spikes. Each of these spikes is approximately 6 dBµV, or two times, lower than the initial frequency spike. In practice, you can obtain a 4-dBµV reduction. In many cases, this reduction is a lifesaver because it helps the circuit pass an EMI test, particularly when bulky ferrites on each cable turn your portable electronic device into a boat anchor.

Figure 1's circuit realizes this technique using a few simple logic gates. You can obtain $x_2(t)$ from the µP timer or the counter by dividing $x_1(t)$ by any number—in this example, 128. Flip-flop IC_1 locks $x_2(t)$ to the crystal oscillator's phase. The XOR gate, IC_2, is the key element. Algebraic multiplication of signals $x_1(t)$ and $x_2(t)$ in **Figure 2a** is equivalent to the XOR function of $x_1(t)$ and $x_2(t)$ when they are "logic" signals. IC_{3A} and IC_{3B} compensate for IC_1's propagation delay. The output of IC_2 routes directly to the clock input of the µP. The resulting signal x(t) experiences two phase shifts over one period of $x_2(t)$ (**Figure 2a**). The first shift of 180° occurs during $x_2(t)$'s transient from logic 0 to logic 1; the second shift of −180° occurs during the transient from logic 1 to logic 0.

From the µP's perspective, the clock signal loses one full period of $x_1(t)$ over one full period of $x_2(t)$. In this example, if you program the µP's internal timer to 127 cycles, the clock counts 128 cycles of the original crystal frequency.

If you use this technique, you can easily predict the µP's clock behavior. For example, sampling with every period of $x_2(t)$ introduces no noise into the ADC's reading. The frequency content of the digital clock and other digital signals contains no low frequencies, such as 50 kHz, so the digital clock does not cause any noise in the analog sections. (DI #2391)

REFERENCE

1. Bolger, Steve, and Samer Omar Darwish, "Use spread-spectrum techniques to reduce EMI," *EDN*, May 21, 1998, pg 141.

TO VOTE FOR THIS DESIGN,
CIRCLE NO. 413

You've got mail

by Gary Kath and Craig Bishop, Scotch Plains, NJ

MANY E-MAIL PROGRAMS provide a "beep" or a pop-up message box signaling the user that a new e-mail message has arrived. If the you are too far from the computer to hear the audible signal or if the monitor is turned off, then you miss the new-mail audible and visual signals. The simple circuit in **Figure 1** (see pg 136) latches on an LED and an audio sounder when an appropriate new audible e-mail signal occurs. The method replaces the normal e-mail sound.wav file with a .wav file of any valid recorded dual-tone multifrequency (DTMF) sound. The circuit listens for the DTMF tone and latches on LED D_1 and the piezoelectric buzzer, P_1. R_1 biases the microphone's FET, and C_1 couples the audio to the M-8870 DTMF-receiver, IC_1 (Teltone Corp, www.teltone.com). IC_1 integrates both bandsplit-filter and decoder functions into an 18-pin DIP.

Resistors R_2 and R_3 configure the on-chip differential amplifier for a gain of 47. The 3.579545-MHz crystal, X_1, provides a precise clock generator for IC_1's digital-counting decoding circuitry. R_4 and C_2 provide an RC guard time to place accept and reject limits on tone duration. IC_1's STD output switches to logic high for the duration of any valid DTMF tone. The NAND gate, IC_{2A}, inverts this logic signal and then directs it to a latch configured with NAND gates IC_{2B} and IC_{2C}. Pushbutton switch S_1 resets the latch. IC_{2D} buffers and inverts the latch's output and drives a 2N2222 transistor, Q_1, thereby turning on the LED and the piezo buzzer. The circuit latches for any valid DTMF tone. You can add additional circuitry to use the M-8870's 4-bit binary outputs, Q_1 to Q_4 if you need to discriminate between DTMF tones. (DI #2399).

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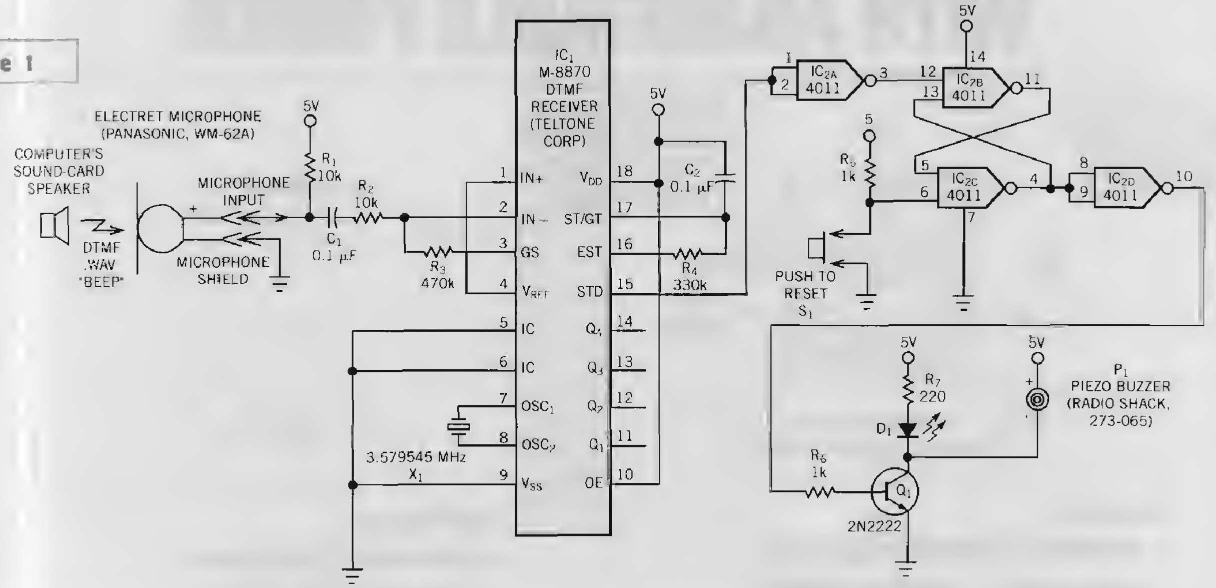
Figure 1



Tired of missing incoming e-mail? This circuit provides a permanent indication of incoming messages.

Circuit provides brownout control of 80C31

By N Kannan, Mediatronix, Pappanamcode, India

In the reset and watchdog-timer circuit in **Figure 1**, IC_1 is a 74HC14 Schmitt-trigger inverter that, with R_1 and C_1, acts as an astable oscillator. The circuit provides an active-high reset for an 80C31 μC. The watchdog trigger (WDT) consists of watchdog-trigger pulses from a port line. At power-on, the voltage on C_1 is 0V, and reset=1. As C_1 charges, reset goes low, and the μC generates watchdog-trigger signals. These ac-coupled pulses periodically turn on Q_1 and charge C_1 to V_{CC}. This action prevents C_1 from discharging through R_1 when reset is low. If the watchdog-trigger pulses stop, Q_1 turns off and C_1 discharges through R_1. reset goes high, resetting the μC. Now, C_1 charges through R_1, and reset goes low after the reset period. D_1 prevents charge-pump action, and D_2 provides a fast discharge path for C_1 when the supply goes down. The Q_2-Q_3 combination acts as a low-voltage reset circuit. When V_{CC} decreases to less than approximately 4.5V, Q_2 turns off and Q_3 turns on, discharging C_1; reset then goes high. The circuit works with voltages as low as 1.5V. During power-up and -down, hysteresis of the inverter provides a clean reset signal. (DI #2400).

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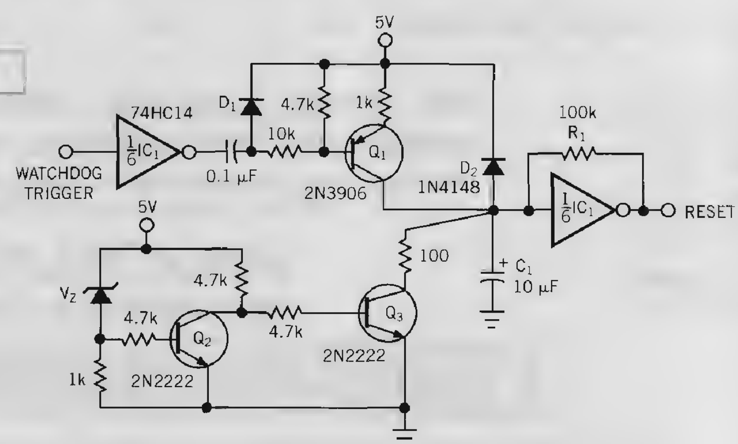
Figure 1



An 80C31 μC receives a clean reset signal from this circuit, which monitors power-up and brownout conditions on the power supply.

Circuit emulates mechanical metronome

Jim Kocsis, Allied Aerospace, South Bend, IN

The circuit in **Figure 1** produces timing signals with a sound like that of a mechanical metronome. IC_1 is a 555 timer that oscillates at approximately 3200 Hz. The two 3-kΩ resistors and the 0.047-μF capacitor set the frequency. IC_2 divides the frequency of IC_1's output by 2. IC_2 produces a square wave with an exact 50% duty cycle. The frequency of the output of IC_2 determines the sound of each beat. A higher frequency yields a sharper sound, like beating on a small drum; a lower frequency produces a deeper sound, like beating on a large drum. You can adjust the sound by changing the values of the 3-kΩ resistors or the 0.047-μF capacitor. The square wave from IC_2 is always present on Pin 1 of IC_5. IC_3 is a low-frequency oscillator that runs from approximately 0.5 to 3 Hz. This oscillator determines the rate or speed of the beat. The two 100-kΩ resistors, the 1-MΩ potentiometer/resistor pair, and the 1-μF capacitor determine the oscillator frequency.

For every rising edge from IC_3, the IC_4 one-shot produces one low-to-high-to-low output pulse. The 30-kΩ resistor and the 0.15-μF capacitor determine the length of IC_4's output pulse. This pulse is approximately 2 msec long with the values shown. The output from IC_4 allows three to four pulses from IC_2 to pass through to the output of IC_5. When IC_5's Pin 2 is high, the pulses from IC_2 appear at IC_5's Pin 3; when Pin 2 is low, no pulses appear at Pin 3. From IC_5's Pin 3, the series of pulses routes to the volume control and then to the power audio amplifier. All the circuitry except IC_6 uses a 5V supply. IC_6 needs a 12V supply to drive the speaker loud enough to hear over the sound of an instrument. If you want a visual indication of the beat, you can connect an npn transistor, with a 470Ω series base resistor, to IC_4's Pin 6. An LED in series with a 470Ω resistor from the collector to 5V produces the visual indication. (DI #2404).

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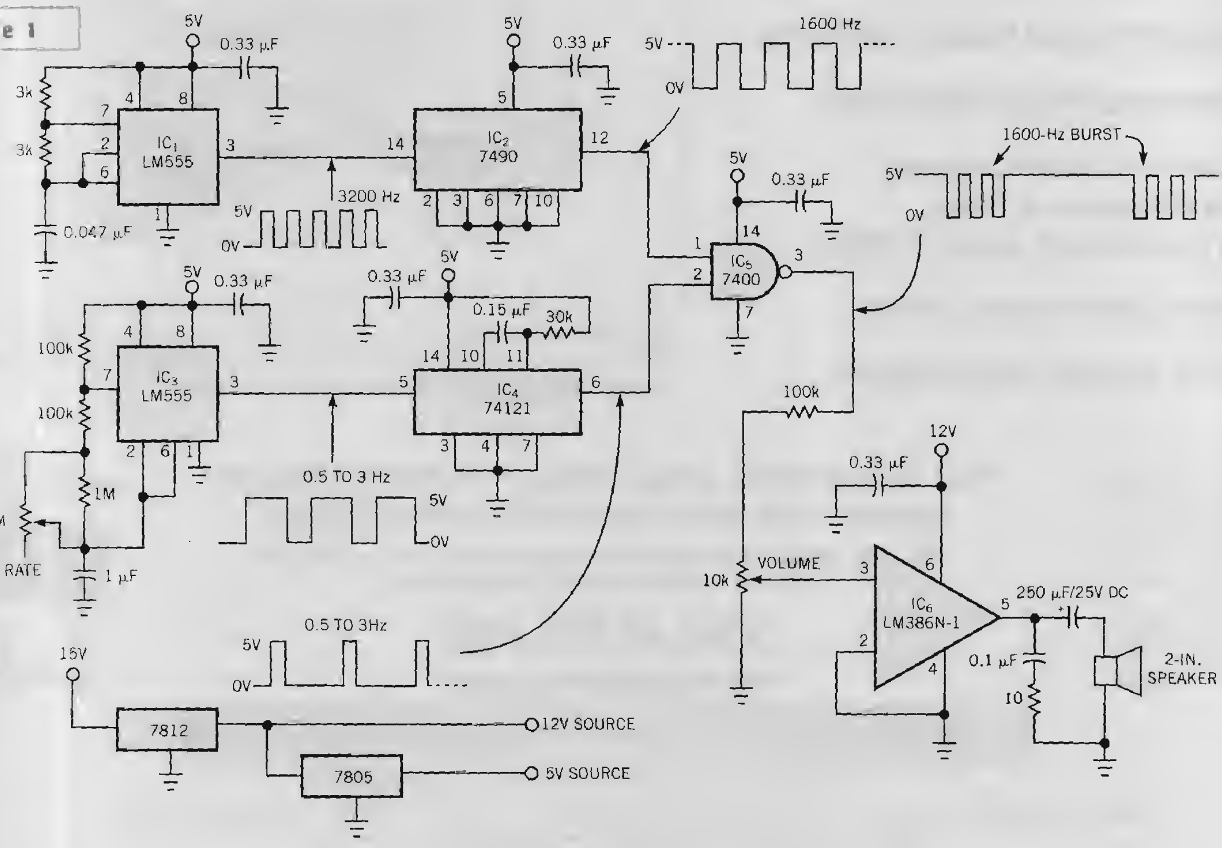
Figure 1



Sounding just like an old-fashioned metronome, this circuit sets the cadence for your music practice.

PC controls light dimmer

Afshin Mellati, Burr-Brown Corp, Tucson, AZ

Using the simple circuit in **Figure 1**, you can control the light intensity in your room or work area from your PC. The heart of the circuit is a low-power D/A converter that converts digital words from a computer's parallel port to analog-voltage signals. To isolate the dc low-voltage part of the circuit from the high-voltage part, the circuit uses an optoisolator, which prevents any direct electrical connection between the two sections. The optoisolator triggers triac T_1, which behaves like a switch. In each power cycle, T_1 switches on, the ac supply voltage connects to the load (lamps), and current starts flowing in the triac. At the end of a half-period, when the current drops to zero, T_1 turns off and awaits another trigger in the opposite direction. This additional trigger occurs in the second half-period of the power cycle. A lower triggering voltage makes T_1 conduct at an earlier point in and stay on for a larger fraction of the cycle. The larger fraction corresponds with transferring more power to the lamp, resulting in a higher intensity.

The output voltage of the D/A converter sets the triggering point. The DAC, after one stage of buffering, provides enough current to drive the optoisolator. IC_3 generates a 2.5V reference; the crystal oscillator and capacitors C_1 through C_4 set the DAC's timing characteristics. The DAC1220 (Burr-Brown Corp, www.burr-brown.com) connects to the parallel port with three wires for serial transfer of the digital codes. The Pascal program of **Listing 1** (pg 142) reads the PC's keyboard; when you press Q or W, the routine increments or decrements a digital code and sends it to the DAC. The DAC then controls the lamp's intensity. Upon power-up, the DAC receives a digital code of zero, which corresponds to a 2.5V output (the reference voltage). You then adjust potentiometer R_3 such that the lamp is half on. Using the keyboard, you can change the light intensity to the desired level. The dc part of the circuit consumes only approximately 5 mA. **Listing 1** is available for downloading from *EDN*'s Web site, www.ednmag.com. Click on "Search Databases" and then enter the Software Center to download the file for Design Idea 2401. (DI #2401).

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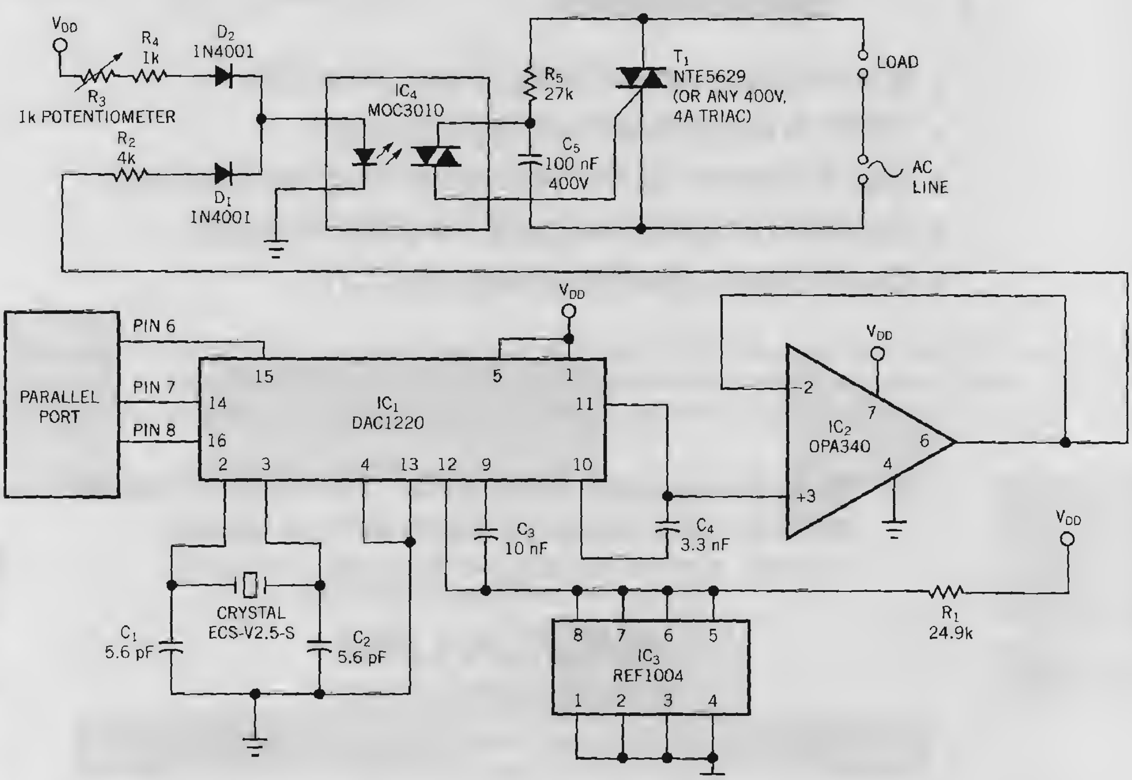
Figure 1



Set your computer area's lighting intensity from the comfort of your swivel chair, using keyboard commands. A simple Pascal routine and some low-cost components do the trick.